查询CAT5132GZ-100TE13供应商

15 Volt Digitally Programmable Potentiometer (DPP™) with 128 Taps and 2-wire Interface

FEATURES

- **Single linear Digitally Programmable Potentiometer**
- **128 Resistor taps**
- **End-to-end resistance of 10kΩ, 50kΩ & 100kΩ**
- **Potentiometer control and memory access via 2-wire interface (I²C-like)**
- **Nonvolatile memory storage for wiper settings**
- **Automatic recall of saved wiper setting at power up**
- **Special increment/decrement instruction mode for automatic trimming adjustments**
- **V_{cc} operation from 2.7 V to 5.5 V**
- **V+ (Analog Voltage Supply) operation from +8 V to +15V**
- **Standby current less than 15 µA**
- **100 year nonvolatile memory data retention**
- **10-pin MSOP package**
- **Operating temperature of -40˚C to + 85˚C**

APPLICATIONS

- **LCD screen adjustment**
- **Volume control**
- **Mechanical potentiometer replacement**
- **Gain adjustment**
- **Line impedance matching**
- **VCOM setting adjustments**

DESCRIPTION

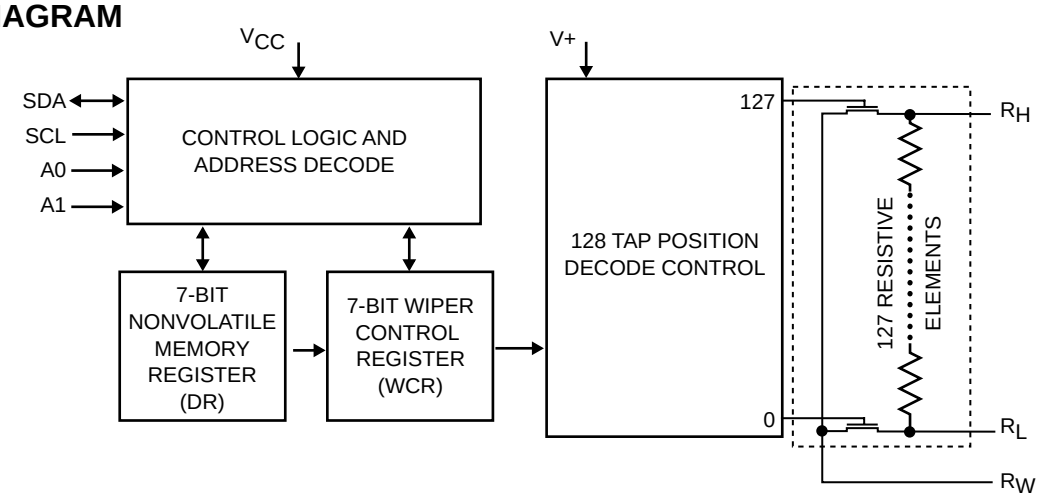
The CAT5132 is a high voltage Digitally Programmable Potentiometer (DPP) integrated with EEPROM memory and control logic to operate in a similar manner as a mechanical potentiometer. The DPP consists of a series of resistive elements connected between two externally accessible end points. The tap points between each resistive element are connected to the wiper output with CMOS switches. A separate 7-bit control register (WCR) independently controls the wiper tap switches for the DPP. Associated with the control register is a 7-bit nonvolatile memory data register (DR) used for storing wiper settings. Writing to the wiper control register or the nonvolatile data register is via a 2-wire serial bus (I^2C-like).

On power-up, WCR is set to mid scale (1000000) and after the Power Supply becomes stable, the contents of the data register (DR) are transferred to the wiper control register (WCR) and the wiper is positioned to that location.

The CAT5132 comes with 2 voltage supply inputs: V_{CC}, the digital supply voltage input and V+, an analog supply voltage input. These inputs allow the V+ to be as much as 10 volts higher than the V_{CC} and allow the DPP terminal values to be as much as 15 volts above ground.

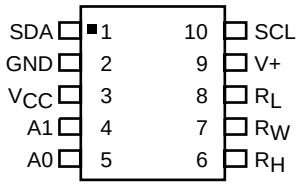
The CAT5132 can be used as a potentiometer or as a two-terminal variable resistor. It is intended for circuit level adjustments. It is supplied standard in the -40°C to +85°C industrial operating temperature range and offered in the 10-pin MSOP package.

BLOCK DIAGRAM



© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

PIN CONFIGURATION

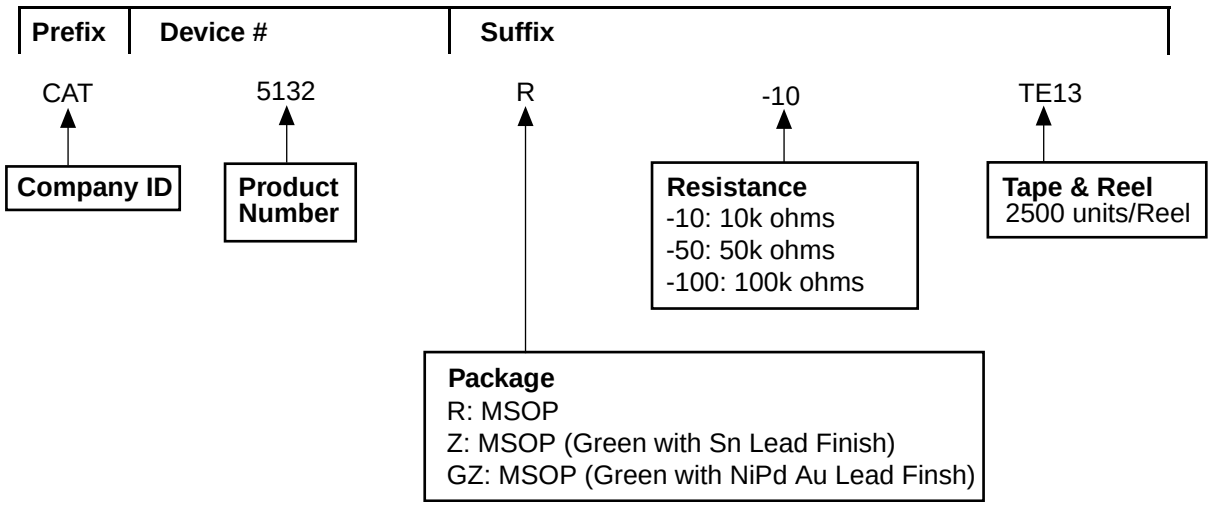


MSOP 10-Pin Package

PIN DESCRIPTION

Pin Number	Name	Description
1	SDA	Serial Data Input/Output - Bidirectional Serial Data pin used to transfer data into and out of the CAT5132. This is an Open-Drain I/O and can be wire OR'd with other Open-Drain (or Open Collector) I/Os.
2	GND	Ground
3	V_{CC}	Digital Supply Voltage (2.7V to 5.5V)
4	A1	Address Select Input to select slave address for 2-wire bus.
5	A0	Address Select Input to select slave address for 2-wire bus.
6	R_H	High Reference Terminal for the potentiometer
7	R_W	Wiper Terminal for the potentiometer
8	R_L	Low Reference Terminal for the potentiometer
9	V+	Analog Supply Voltage for the potentiometer (+8.0V to 15.0V)
10	SCL	Serial Bus Clock input for the 2-wire Serial Bus. This clock is used to clock all data transfers into and out of the CAT5132

ORDERING INFORMATION



Notes:
1. The device used in the above example is a CAT5132R-10TE13 (MSOP, 10k ohms, Tape & Reel).
2. The Industrial Temperature range of -40˚C to +85˚C is standard on the above product.

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias.....-55˚C to +125˚C

Storage Temperature ..... -65˚C to +150˚C

Voltage on any SDA, SCL, A0 & A1 pins with respect to Ground (1)(2) ..... -2.0V to V_{CC} + 2.0V

Voltage on R_H, R_L & R_W Pins with respect to Ground ..... -2.0V to "V+" + 1.0V

V_{CC} with respect to Ground ..... -2.0V to 7.0V

V+ with respect to Ground ..... -2.0V to 16.0V

Wiper Current (10 sec) ..... ±6mA

Lead Soldering temperature (10 sec) .....+300˚C

RECOMMENDED OPERATING CONDITIONS

V_{CC} = +2.7V to +5.5V
V+ = 8.0V to +15V
Operating Temperature Range: -40˚C to +85˚C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

POTENTIOMETER CHARACTERISTICS

(Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
R_{POT}	Potentiometer Resistance (100kΩ)			100		kΩ
R_{POT}	Potentiometer Resistance (50kΩ)			50		kΩ
R_{POT}	Potentiometer Resistance (10kΩ)			10		kΩ
R_{TOL}	Potentiometer Resistance Tolerance				±20	%
	Power Rating	25• C			50	mW
I_W	Wiper Current				±3	mA
R_W	Wiper Resistance	I_W = ±1mA @ V+ = 12V		70	150	Ω
		I_W = ±1mA @ V+ = 8V		110	200	Ω
V_{TERM}	Voltage on R_W, R_H or R_L	GND = 0V; V+ = 8V to 15V	GND		V+	V
RES	Resolution			0.78		%
A_{LIN}	Absolute Linearity (2)	$R_{W(n)(actual)}$ - $R_{W(n)(expected)}$ (5)			±1	LSB (4)
R_{LIN}	Relative Linearity (3)	$R_{W(n+1)}$ - [$R_{W(n)}$+LSB](5)			±0.5	LSB (4)
TC_{RPOT}	Temperature Coefficient of R_{POT}	(1)		±300		ppm/• C
TC_{Ratio}	Ratiometric Temperature Coefficient	(1)			30	ppm/• C
$C_H/C_L/C_W$	Potentiometer Capacitances	(1)		10/10/25		pF
fc	Frequency Response	R_{POT} = 50kΩ		0.4		MHz

Notes:
1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
3. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer.
4. LSB = (R_{HM} - R_{LM})/127; where R_{HM} and R_{LM} are the highest and lowest measured values on the wiper terminal.
5. n = 1, 2, ..., 127

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

D.C. ELECTRICAL CHARACTERISTICS

(Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Power Supply Current (Volatile Write/Read)	F_{SCL} = 400kHz, SDA Open, V_{CC} = 5.5V, Input = GND		1	mA
I_{CC2}	Power Supply Current (Nonvolatile WRITE)	F_{SCL} = 400kHz, SDA Open, V_{CC} = 5.5V, Input = GND		3.0	mA
$I_{SB(VCC)}$	Standby Current (V_{CC} = 5V)	V_{IN} = GND or V_{CC} , SDA = V_{CC}		5	µA
$I_{SB(V+)}$	V+ Standby Current	V_{CC} = 5V, V+ = 15V		10	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		10	µA
V_{IL}	Input Low Voltage		-1	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 1.0	V
V_{OL1}	Output Low Voltage (V_{CC} = 3.0)	I_{OL} = 3mA		0.4	V

CAPACITANCE

T_A = 25˚C, f = 1.0MHz, V_{CC} = 5.0V

Symbol	Parameter	Test Conditions	Min	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V (1)		8	pF
C_{IN}	Input Capacitance (A0, A1, SCL)	V_{IN} = 0V (1)		6	pF

A.C. CHARACTERISTICS

Symbol	**Parameter** (see Fig. 1)	**V_{CC} = 2.7 - 5.5V**		Units
		Min	Max	
F_{SCL}	Clock Frequency		400	kHz
T_I (1)	Noise Suppression Time Constant at SCL & SDA Inputs		50	ns
t_{AA}	SLC Low to SDA Data Out and ACK Out		1	µs
t_{BUF} (1)	Time the bus must be free before a new transmission can start	1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
t_{LOW}	Clock Low Period	1.2		µs
t_{HIGH}	Clock High Period	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		ns
t_R (1)	SDA and SCL Rise Time		0.3	µs
t_F (1)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Conditions Setup Time	0.6		µs
t_{DH}	Data Out Hold Time	100		ns

Notes:

1. This parameter is tested initially and after a design or process change that affects the parameter.

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

POWER UP TIMING (1)(2)

Symbol	Parameter	Min	Max	Units
t_{PUR}	Power-up to Read Operation		1	ms
t_{PUW}	Power-up to Write Operation		1	ms

XDCP TIMING

Symbol	Parameter	Min	Max	Units
t_{WRPO}	Wiper Response Time After Power Supply Stable	5	10	µs
t_{WRL}	Wiper Response Time After Instruction Issued	5	10	µs

WRITE CYCLE LIMITS

Symbol	Parameter	Min	Max	Units
t_{WR}	Write Cycle Time (see Fig. 2)		5	ms

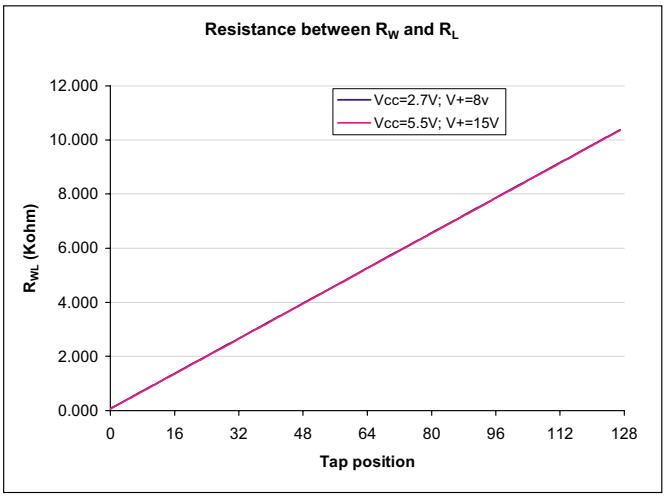
The write cycle is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

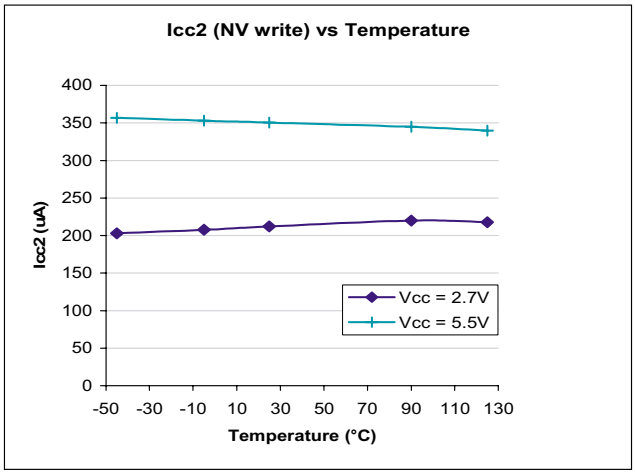
RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END} (1)	Endurance	MIL-STD-883, Test Method 1033	100,000		Cycles/Byte
T_{DR} (1)	Data Retention	MIL-STD-883, Test Method 1008	100		Years
V_{ZAP} (1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000		Volts
I_{LTH} (1)	Latch-Up	JEDEC Standard 17	100		mA

Notes:
1. This parameter is tested initially and after a design or process change that affects the parameter.
2. t_{PUR} and t_{PUW} are the delays required from the time VCC is stable until the specified operation can be initiated.

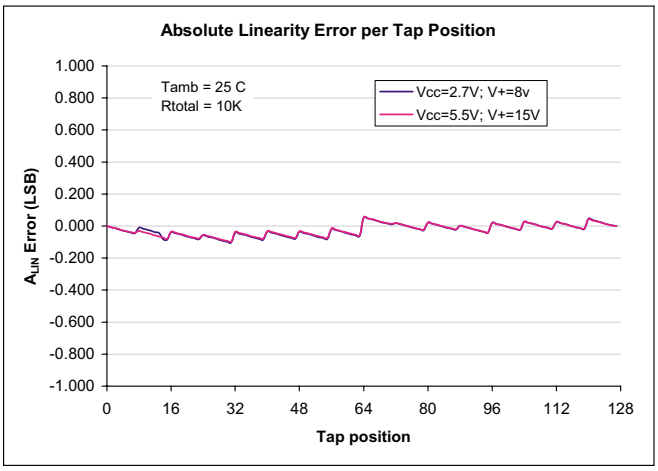
TYPICAL PERFORMANCE CHARACTERISTICS

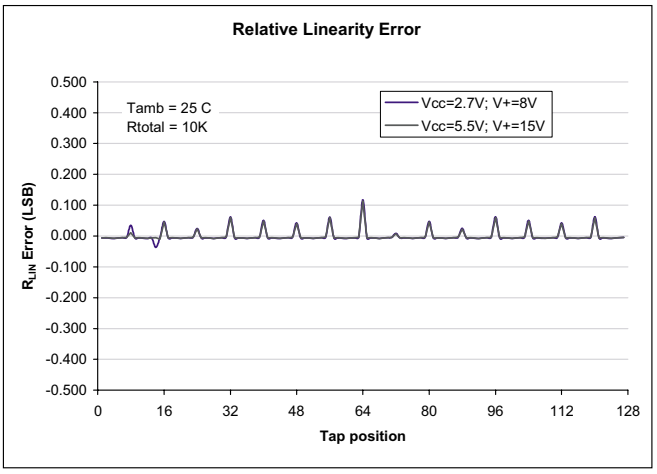




© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

TYPICAL PERFORMANCE CHARACTERISTICS (CONT)





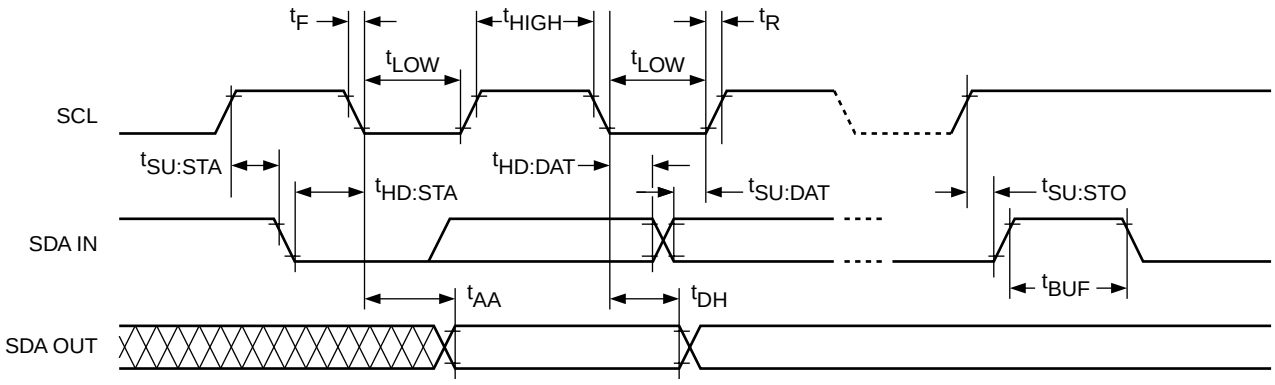


Figure 1. Bus Timing

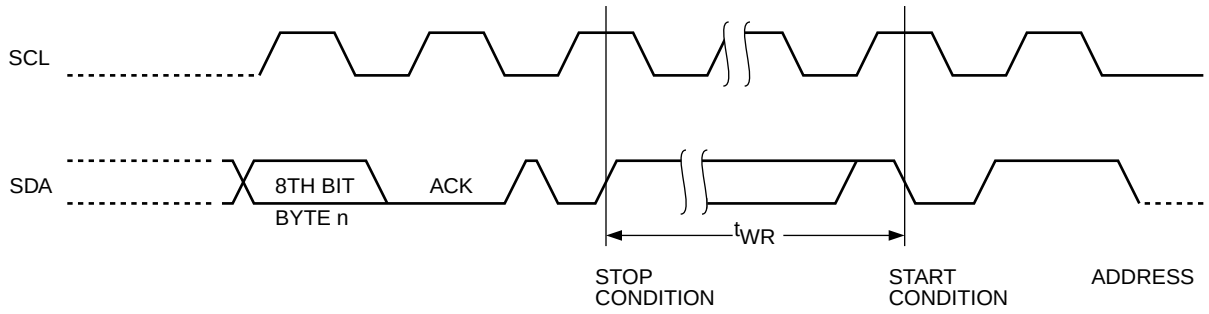


Figure 2. Write Cycle Timing

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

SERIAL BUS PROTOCOL

The following defines the features of the 2-wire bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the CAT5132 will be considered a slave device in all applications.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT5132 monitors the SDA and SCL lines and will not respond until this condition is met (see Fig. 3).

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition (see Fig. 3).

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data (see Fig. 4).

The CAT5132 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT5132 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT5132 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT5132 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address. If the CAT5132 is still busy with the write operation, no ACK will be returned. If the CAT5132 has completed the write operation, an ACK will be returned and the host can then proceed with the next instruction operation.

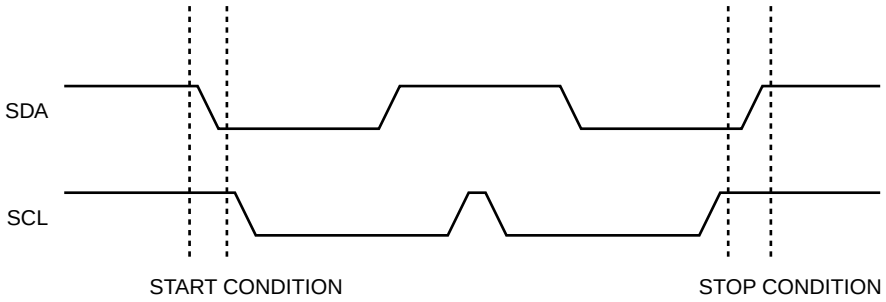


Figure 3. Start/Stop Condition

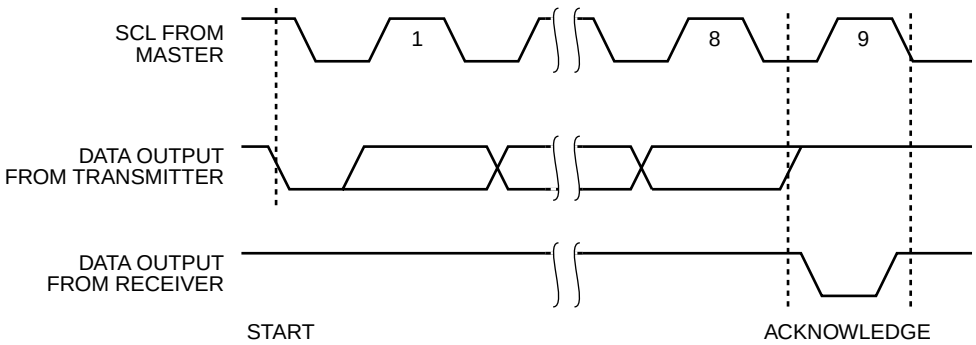


Figure 4. Acknowledge Condition

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

DEVICE DESCRIPTION

Access Control Register

The volatile register WCR and the non-volatile register DR of CAT5132 are accessed only by addressing the volatile Access Register AR first, using the 3 byte I^2C interface for all read and write operations (see Table 1). The first byte is the slave address/instruction byte (see details below). The second byte contains the address (02h) of the AR register. The data in the third byte controls which register WCR (80h) or DR (00h) is being addressed (see Figure 5).

Slave Address Instruction Byte Description

The first byte sent to the CAT5132 from the master processor is called the Slave/DPP Address Byte. The most significant five bits of the slave address are a device type identifier. These bits for the CAT5132 are fixed at 01010 (refer to Table 2).

The next two bits, A1 and A0, are the internal slave address and must match the physical device address which is defined by the state of the A1 and A0 input pins to successfully address the CAT5132. Only the device with slave address matching the input byte will be accessed by the master. This allows up to 4 devices to reside on the same bus. The A1 and A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or Ground.

The last bit is the READ/WRITE bit and determines the function to be performed. If it is a “1” a read command is initiated and if it is a “0” a write is initiated. For the AR register only write is allowed.

After the Master sends a START condition and the slave address byte, the CAT5132 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address.

Table 1. Access Control Register

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address - 02h									WCR(80h) / DR (00h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	SP
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	SP

Table 2. Byte 1 Slave Address and Instruction Byte

Device Type Identifier					Slave Address		Read/$\overline{\text{Write}}$
ID4	ID3	ID2	ID1	ID0	A1	A0	R/$\overline{W}$
0	1	0	1	0	X	X	X
(MSB)							(LSB)

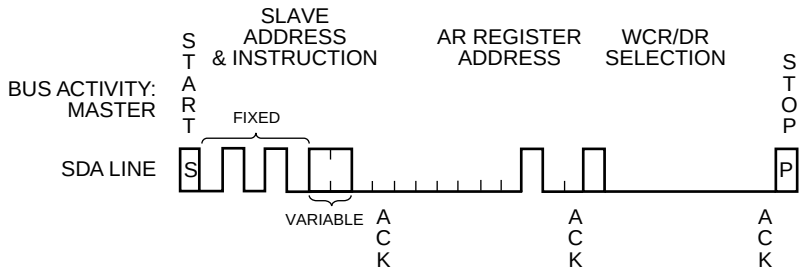


Figure 5. Access Register Addressing Using 3 Bytes

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

Wiper Control Register (WCR) Description

The CAT5132 contains a 7-bit Wiper Control Register which is decoded to select one of the 128 switches along its resistor array. The WCR is a volatile register and is written with the contents of the nonvolatile Data Register (DR) on power-up. The Wiper Control Register loses its contents when the CAT5132 is powered-down. The contents of the WCR may be read or changed directly by the host using a READ/WRITE command after addressing the WCR (see Table 1 to access WCR). Since the CAT5132 will only make use of the 7 LSB bits (The first data bit, or MSB, is ignored) on write instructions and will always come back as a “0” on read commands.

A write operation (see Table 3) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a data byte and a STOP condition. After each of the three bytes the CAT5132 responds with an acknowledge. At this time the data is written only to volatile registers, then the device enters its standby state.

Table 3. WCR Write Operation

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address - 02h									WCR(80h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	WCR address - 00h								ACK	data byte								ACK	STOP
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	X	X	X	X	X	X	X	X	A	SP

An increment operation (see Table 4) requires a Start condition, followed by a valid increment address byte (01011), a valid address byte 00h. After each of the two bytes, the CAT5132 responds with an acknowledge. At this time if the data is high then the wiper is incremented or if the data is low the wiper is decremented at each clock. Once the stop is issued then the device enters its standby state with the WCR data as being the last inc/dec position. Also, the wiper position does not roll over but is limited to min and max positions.

Table 4. WCR Increment/Decrement Operation

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address - 02h									WCR(80h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	WCR address - 00h								ACK	increment (1) / decrement (0) bits									STOP
ST	0	1	0	1	1	0	0	0	A	0	0	0	0	0	0	0	0	A	1	1	1	1	0	0	0	0		SP

A read operation (see Table 5) requires a Start condition, followed by a valid slave address byte for write, a valid address byte 00h, a second START and a second slave address byte for read. After each of the three bytes, the CAT5132 responds with an acknowledge and then the device transmits the data byte. The master terminates the read operation by issuing a STOP condition following the last bit of Data byte.

Table 5. WCR Read Operation

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address - 02h									WCR(80h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	WCR address - 00h								
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	

START	slave address byte									data byte									STOP
ST	0	1	0	1	0	0	0	1	A	0	X	X	X	X	X	X	X		SP

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

Data Register (DR)

The Data Register (DR) is a nonvolatile register and its contents are automatically written to the Wiper Control Register (WCR) on power-up. It can be read at any time without effecting the value of the WCR. The DR, like the WCR, only stores the 7 LSB bits and will report the MSB bit as a “0”. Writing to the DR is performed in the same fashion as the WCR except that a time delay of up to 5ms is experienced while the nonvolatile store operation is being performed. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. The WCR is also written during a write to DR. After a DR WRITE is complete the DR and WCR will contain the same wiper position.

To write or read to the DR, first the access to DR is selected, see table 1 then the data is written or read using the following sequences.

A write operation (see Table 6) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a data byte and a STOP condition. After each of the three bytes the CAT5132 responds with an acknowledge. At this time the data is written both to volatile and non-volatile registers, then the device enters its standby state.

Table 6. DR Write Operation

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address - 02h									DR(00h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	DR address - 00h								ACK	data byte								ACK	STOP
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	X	X	X	X	X	X	X	X	A	SP

A read operation (see Table 7) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a second Start and a second slave address byte for read. After each of the three bytes the CAT5132 responds with an acknowledge and then the device transmits the data byte. The master terminates the read operation by issuing a STOP condition following the last bit of Data byte.

Table 7. DR Read Operation

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address - 02h									DR(00h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	DR address - 00h								
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	

START	slave address byte									data byte									STOP
ST	0	1	0	1	0	0	0	1	A	0	X	X	X	X	X	X	X		SP

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

POTENTIOMETER OPERATION

Power-On

The CAT5132 is a 128-position, digital controlled potentiometer. At power-up the device turns on at the mid-point wiper location (64) until the wiper register can be loaded with the nonvolatile memory location previously stored in the device. After the nonvolatile memory data is loaded into the wiper register the wiper location will change to the previously stored wiper position.

The end-to-end nominal resistance of the potentiometer has 128 contact points linearly distributed across the total resistor. Each of these contact points is addressed by the 7 bit wiper register which is decoded to select one of these 128 contact points.

Each contact point generates a linear resistive value between the 0 position and the 127 position. These values can be determined by dividing the end-to-end value of the potentiometer by 127. In the case of the 10kΩ potentiometer~79Ω is the resistance between each wiper position. However in addition to the ~79Ω for each resistive segment of the potentiometer, a wiper resistance offset must be considered. Table 8 shows the effect of this value and how it would appear on the wiper terminal.

This offset will appear in each of the CAT5132 end-to-end resistance values in the same way as the 10kΩ example. However resistance between each wiper position for the 50kΩ version will be ~395Ω and for the 100kΩ version will be ~790Ω.

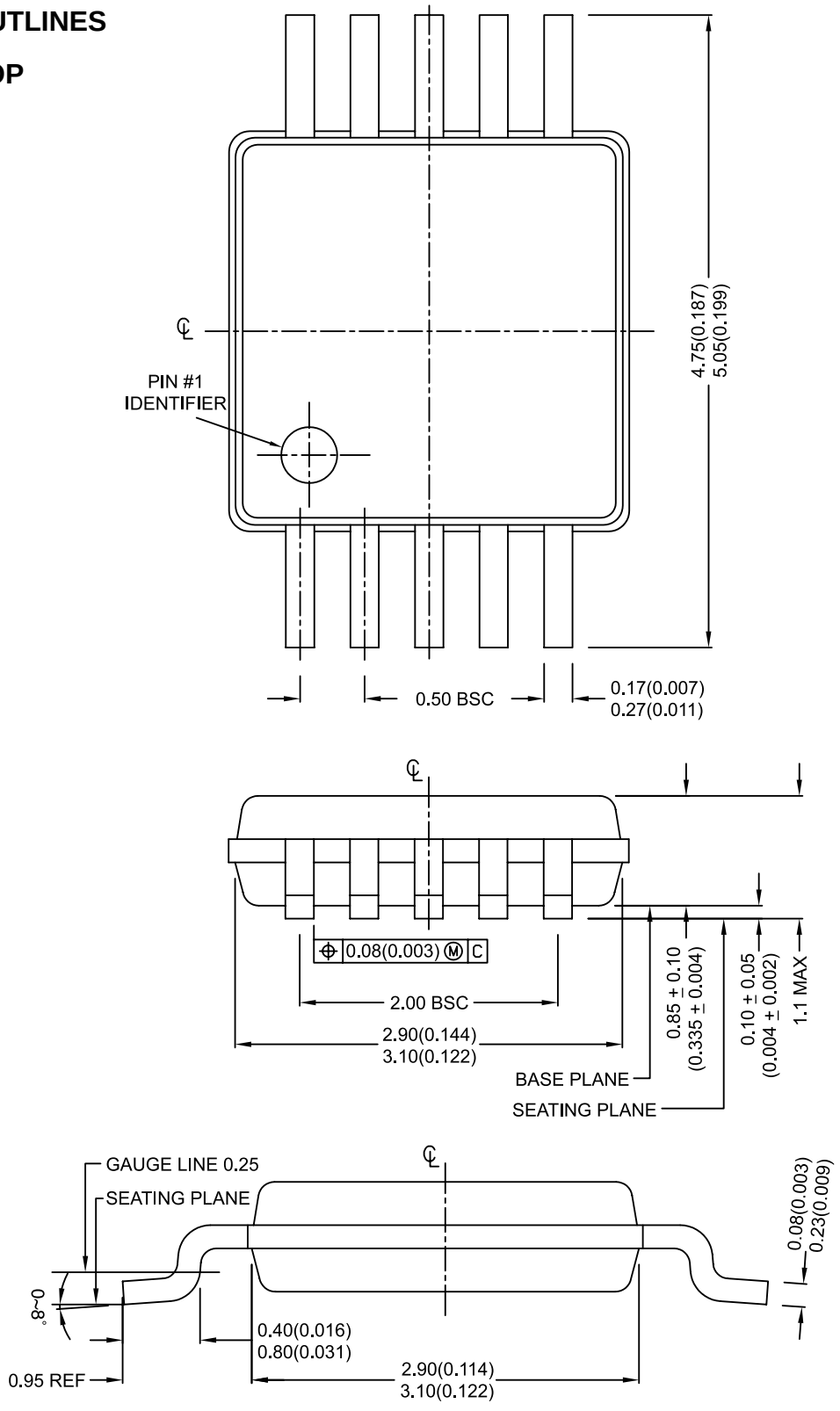
Table 8. Potentiometer Resistance and Wiper Resistance Offset Effects

Position	Typical R_W to R_L Resistance for 10kΩ DPP	
00	70Ω or	0Ω + 70Ω
01	149Ω or	79Ω + 70Ω
63	5,047Ω or	4,977Ω + 70Ω
127	10,070Ω or	10,000Ω + 70Ω
Position	**Typical R_W to R_H Resistance for 10kΩ DPP**	
00	10,070Ω or	10,000Ω + 70Ω
64	5,047Ω or	4,977Ω + 70Ω
126	149Ω or	79Ω + 70Ω
127	70Ω or	0Ω + 70Ω

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

PACKAGE OUTLINES

10-LEAD MSOP



NOTES:
1) LEADFRAME MATERIAL: C7025 (THICKNESS: 0.15MM).
2) BOTH PACKAGE LENGTH & WIDTH DO NOT INCLUDE MOLD FLASH.
3) FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.10MM.
4) UNREMOVED FLASH BETWEEN LEADS & PACKAGE END FLASH SHALL NOT EXCEED 0.15MM FROM BOTTOM BODY.
5) CONTROLLING DIMENSION: MM (INCH).

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

REVISION HISTORY

Date	Rev.	Reason
09/12/2005	00	Initial Issue

Copyrights, Trademarks and Patents
Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:

DPP ™ AE^2 ™ MiniPot™

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products. For a complete list of patents issued to Catalyst Semiconductor contact the Company's corporate office at 408.542.1000.

CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.

Catalyst Semiconductor, Inc.
Corporate Headquarters
1250 Borregas Avenue
Sunnyvale, CA 94089
Phone: 408.542.1000
Fax: 408.542.1200
www.caalyst-semiconductor.com

Publication #: 25092
Revison: 00
Issue date: 09/12/05